

LA-UR-00-2356

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BPM Analog Front-End Electronics Based on the AD8307 Log Amplifier¹

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Abstract. Beam position monitor (BPM) signal-processing electronics utilizing the Analog Devices AD8307 logarithmic amplifier has been developed for the Low Energy Demonstration Accelerator (LEDA), part of the Accelerator Production of Tritium (APT) project at Los Alamos. The low-pass filtered 350 MHz fundamental signal from each of the four microstrip electrodes in a BPM is “detected” by an AD8307 log amp, amplified and scaled to accommodate the 0 to +5V input of an analog-to-digital (A/D) converter. The resultant four digitized signals represent a linear power relationship to the electrode signals, which are in turn related to beam current and position. As the AD8307 has a potential dynamic range of approximately 92 dB, much attention must be given to noise reduction, sources of which can be digital signals on the same board, power supplies, inter-channel coupling, stray RF and others. This paper will describe the operational experience of this particular analog front-end electronic circuit design.

CIRCUIT DESCRIPTION

Referring to the block diagram in Figure 1, signals from the four electrodes of the beam position monitors are low-pass filtered and input to the AD8307 log amplifier through a transformer balun, which is required because of the differential inputs with an impedance of 1 k Ω shunted by 1.4 pf to common. We initially tried to create a narrow-band matching circuit according to the AD8307 data sheet to provide the impedance match, but found it much more difficult to implement with the input filter than the transformer broadband match. A minicircuits ERA-5SM pre-amplifier was installed between the filter and the transformer to adjust the signal high-end for the log amp’s maximum input of approximately 17 dBm, thereby obtaining the greatest signal to noise ratio and dynamic range (approximately 92 dB is specified for the AD8307).

The output of the log amp is a 2 μ A/dB_{input} current, which develops a 25 mV/dB_{input} voltage across a 12.5 k Ω internal resistor. We chose to use an external parallel 12.5 k Ω resistor that increases the frequency response (from approximately 1 MHz) with the tradeoff of reducing the output voltage and increasing output ripple. The log amp output is then amplified, scaled and offset-adjusted by two following AD8041 amplifier stages for a 0 – 5 V range. The signal is then low-pass filtered to a 200 KHz band-width and fed into an AD9241 14-bit analog to digital converter. Since the resolution of 14 bits is 1 part in 16,384, providing 84 dB dynamic range, only 12 bits are used, giving a range of 72 dB which is sufficient for our requirements.

¹ This work supported by the U.S. Department of Energy.

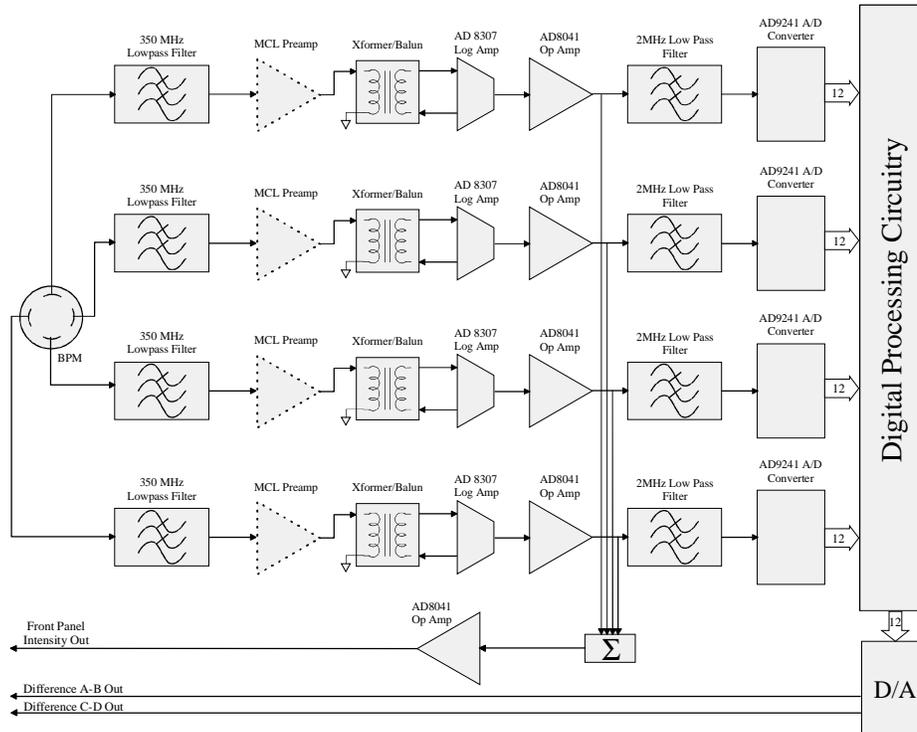


Figure 1. AFE Block Diagram

CIRCUIT SHORTCOMINGS

We initially tested the analog part of the Analog Front End (AFE) board using lab power supplies and without the digital circuitry installed. Using a LabVIEW automated test set-up, the circuit provided a very linear output over a 70-75 dB range (Figure 2).

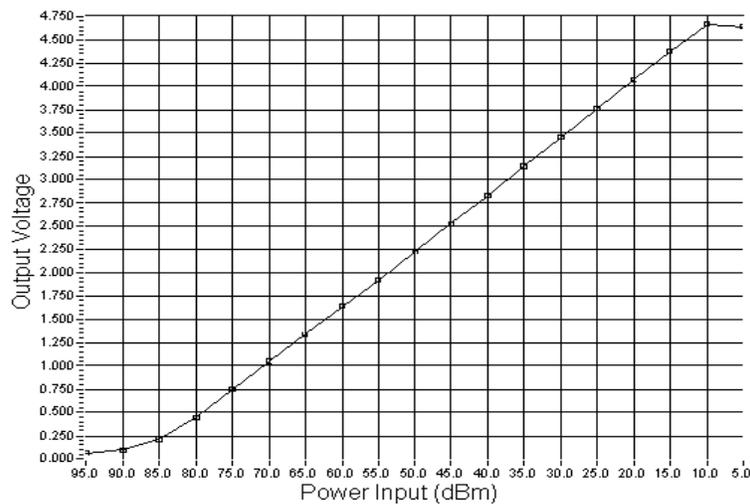


Figure 2. Analog section Dynamic Range

When we subsequently installed the digital components and used the on-board power supplies, however, the dynamic range degraded appreciably to around 60 dB. Figure 3 shows this degradation with the now-digitized output.

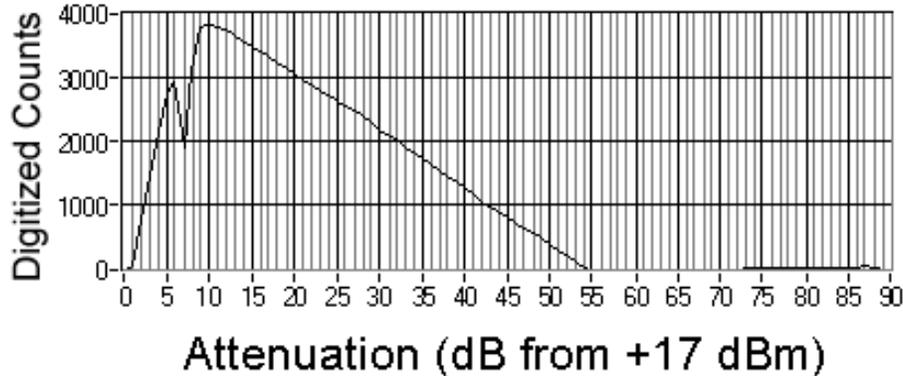


Figure 3. Degraded Dynamic Range – about 45 dB

Noise generated by the digital circuits could easily be coupled into the analog section as the power ($\pm 5V$, $\pm 15V$) and ground planes of the analog and digital circuits are either common or partially overlapping, which is generally considered poor technique [6].

We experienced a number of log amp failures (the first stage or two blown-out) which only occurred with the MCL ERA-5sm pre-amplifier in the circuit. At this time, the exact mechanism of this failure is unknown, but it is thought to be due to power-up transients getting through the pre-amp power supply decoupling circuit and amplified to greater than the maximum allowable input of the log amp.

Another problem, although not strictly involving the analog section of the circuit, was due to the way that Analog Devices labeled the digital outputs on the AD9241 analog to digital converter. The output bits are labeled from the least significant bit to most significant bit as bit 14 through 1, respectively. This caused a reversal of the data word as input to the FPGA's and lookup table correction factors, necessitating subsequently programming into the FPGA's an algorithm for reversing the data order.

CURRENT SOLUTIONS

The noise which was coupling from the power planes to the circuit, was attenuated in two ways: First, since the power for the analog circuits was routed through a separate path and connectors, it was relatively easy to retro-fit a $10\ \mu f$ and $0.1\ \mu f$ bypass capacitor on each of the supply lines. Second, it was determined that the input power from the largest probes (and therefore a lower power output at beam center) would be just adequate without inserting the ERA-5 pre-amp. Removing this amplifier also helped to further reduce the noise sufficiently to allow the circuit to meet the minimum required dynamic range for this phase of LEDA.

FUTURE IMPROVMENTS

As we continue to use this circuit in the beam halo experiment, the follow-on experiment to characterization of the LEDA RFQ, and the Isotope Production Facility at LANSCE, the need for selectable pre-amplification and noise reduction becomes paramount. We are looking closely into power-and-ground-plane separation methods, trace routing, and circuit shielding of the low-level front ends, for both inter-channel coupling and external EMI. Additionally, good low noise pre-amps with internal power supply decoupling are being considered.

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